

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-21. (Canceled).

22. (Currently amended) A method comprising:
~~detecting a command to transition a host processor to a low power state;~~
~~writing a first sleep type to a first register to that controls at least part of a~~
~~specify transition of a system to the a low power system state for~~
~~the host processor, wherein the first sleep type is not recognized by~~
~~at least part of the system;~~
~~notifying a microcontroller of the transition command to the host~~
~~processor; changing a power state of a microcontroller within the~~
~~system in response to the writing of the first sleep type;~~
~~identifying the first sleep type as a substitute for a second sleep type~~
~~recognized by the at least part of the system, and writing the~~
~~second sleep type to a second register that controls at least part of~~
~~the transition of the system to the low power system state; and~~
~~pointing the host processor to an instruction that, when executed, causes~~
~~the host processor to write a second sleep type to a second register~~
~~that controls the power state of the microcontroller, wherein said~~
~~second sleep type is not recognized by the microcontroller; and~~
~~changing the power state of the microcontroller system in response to the~~
~~writing of the second sleep type.~~

23. (Currently amended) The method of claim 22, wherein changing the power state of the microcontroller system comprises changing the power state of the microcontroller to a like-low power device state to that of the host processor.

24. (Currently amended) The method of claim 22, wherein changing the power state of the microcontroller system comprises shutting down the microcontroller.

25. (Original) The method of claim 22, wherein the computer system has at least one peripheral device, and further including notifying the peripheral device to perform a custodial function.

26. (Currently amended) A memory device containing code that is executable in a computer system and causes the computer system to:

~~detect a command to transition a host processor to a low power state;~~
~~write a first sleep type to a first register to specify that controls at least part of a transition of a system to the a low power system state, for the host processor wherein the first sleep type not is recognized by at least part of the system;~~
~~notify a microcontroller of the transition command to the host processor; change a power state of a microcontroller within the system in response to the writing of the first sleep type;~~
~~identify the first sleep type as a substitute for a second sleep type recognized by the at least part of the system, and write the second sleep type to a second register that controls at least part of the transition of the system to the low power system state; and~~
~~point the host processor to an instruction that, when executed, causes the host processor to write a second sleep type to a second register that controls the power state of the microcontroller, wherein said second sleep type is not recognized by the microcontroller; and~~
~~change the power state of the microcontroller system in response to the writing of the second sleep type.~~

27. (Currently amended) The memory device of claim 26, wherein the memory device code causes the computer system to perform the act of changing

the power state of the microcontroller to a like low power device state to the host processor.

28. (Original) The memory device of claim 26, wherein the memory device code causes the computer system to perform the act of shutting down the microcontroller.

29. (Original) The memory device of claim 26, wherein the computer system includes at least one peripheral device, and wherein the memory device causes the computer system to perform the act of notifying the peripheral device to perform a custodial function.

30. (Currently amended) The method of claim 22 further comprising transitioning out of the low power state and executing said instruction writing the first sleep type to the second register.

31. (Currently amended) The memory device of claim 26 wherein the memory device code causes the computer system to perform the acts of transitioning out of the low power state and executing said instruction writing the first sleep type to the second register.